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"NUMERICAL SIMULATION OF THE ELECTRICAL CHARACTERISTICS OF NANOSCALE TG n-FinFET WITH THE VARIATION OF GATE DIELECTRIC MATERIALS"

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ABSTRACT

We have been simulated the electrical characteristics of a 3-D silicon on insulator (SOI)triple gate (TG) nFinFET with a channel length of 5nm. Different gate dielectric materials have been used in this simulation with the help of SILVACO TCAD tools. The gate materials are SiO_2, Si_3N_4, ZrO_2, HfO_2 and TiO_2. The electrical characteristics such as threshold voltage, ON current (I_{ON}), OFF current (I_{OFF}), ratio of On-Off current, Subthreshold slope (SS), drain induced barrier lowering (DIBL) and transconductance (g_m) have been simulated. After analyzing the simulations, we have seen that high permittivity (k=40) of gate material (TiO_2) gives improve values ofthreshold voltage, subthreshold swing, on-off current ratio, transconductance in comparison with other dielectric SiO_2, Si_3N_4, ZrO_2, and HfO_2.Finally, the high k dielectric materials have a better option in the fabrication of TG FinFET device in future.

KEYWORDS: nFinFET, Gate Oxide, Channel Length & Silvaco TCAD

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Original Article

INTRODUCTION

The number of components in ICs drastically increasing day by day. Due to these reasons, the channel length is decreasing. The channel length and channel material have a great influence on the electrical characteristics of FinFET devices. We tried to find the influence of gate oxide materials on the electrical characteristics such as subthreshold swing (SS), threshold voltage, I_{ON}/I_{OFF}, drain induced barrier lowering (DIBL) and transconductance are simulated. Many researches have been done demonstrating to improve SS, DIBL, I_{ON}/I_{OFF} and transconductance [1].In this simulation, various dielectric materials have been used. The gate materials are SiO_2, Si_3N_4, ZrO_2, HfO_2 and TiO_2 and channel length is considered as 5nm.

Nowadays, most of the semiconductor industries introduced silicon on insulator (SOI) substrate to minimize parasitic capacitance and to improve the electrical characteristics of the devices. Among all the parameters, gate materials plays an important role in observing the electrical characteristics of FinFET.

The materials which have low dielectric constant such as silicon nitride Si_3N_4 and silicon dioxide $SiO_2$are leads to leakage currents. So the CMOS industries are moved to medium k materials such as zirconium dioxide ZrO_2or hafnium dioxide HfO_2 to decrease the stress on the thickness of the gate materials. However, the permittivity of used gate materials is not so much rich to fulfill the more high capacitance densities. The researcher is using high dielectric constant called "high k" materials such as titanium dioxide Ta_2O_5 and titanium dioxide TiO_2. So the high

k dielectric materials are replacing the silicon dioxide SiO_2 for the gate of SOI triple gate nFinFET devices which provides good capacitance, better ON current, lower leakage current, providing lower power dissipation and more breakdown voltage [2].

One of the most important parameters for multiage FinFET is Effective Oxide Thickness (EOT). This parameter may be calculated according to the expression 1, it is possible to increase the oxide thickness while keeping the same capacity value by increasing the dielectric constant of the material [2-7].

$$EOT = tsio_2\left(\frac{ksio2}{khigh.k}\right) t_{high.k} \quad .(1).$$

In this paper, we examine various electrical characteristics related to the different values of permittivity of the gate dielectric materials such as SiO_2, Si_3N_4, ZrO_2, $HfO_2$and TiO_2in the TG nFinFET device.

Device Structure

The schematic 3-D structure simulated by Silvaco TCAD simulation is shown in Figure 1. In Silvaco TCAD tools, DEVEDIT is used to design the device structure and ATLAS is used to simulate the graph. Five different dielectric materials have been used as a gate dielectric. The permittivity of these materials is shown in below Table-1 and table-2 shows the different parameters used in the simulated device TG nFinFET.

Table 1: The Permittivity (k) Values of the Gate Materials

Name of the Gate Dielectric	Permittivity (k)
SiO_2	3.9
Si_3N_4	9.5
ZrO_2	29
HfO_2	25
TiO_2	40

Table2: Parameters of Symmetrical SOI nFinFET

Designation	Value
Drain and source length	10nm
Channel length	5nm
Gate oxide length	5nm
Lateral oxide length	1nm
Silicon thickness	4nm
Fin Height	10nm
Buried oxide thickness	15nm
Substrate thickness	10nm
Channel concentration	$10^{16}[cm^{-3}]$
Drain and source concentration	$10^{20}[cm^{-3}]$
Work function	4.71eV

The finFETN device structure depends on the vertical silicon fin characterized by the fin length and fin height.

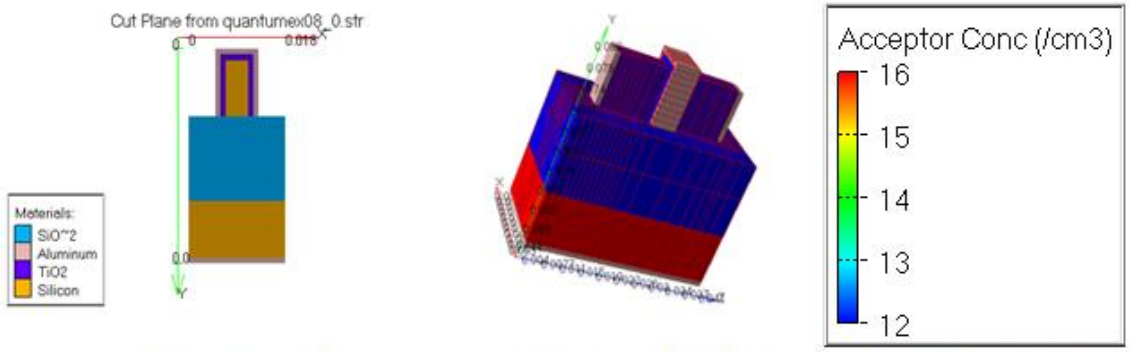

Figure 1: Illustrates the Device Structure, Materials, Cut Plane view and Carrier Concentration of a TG nFinFET in 3-D with a Channel Length of 5nm.

The threshold voltage of a Multi Gate Field-Effect Transistor device can be calculated by the following expression [8,11]:

$$V_{th} = \Phi_{ms} + 2\Phi_f + \frac{Qd}{Cox} + \frac{Qss}{Cox} + V_{in} \quad (2)$$

$$\Phi_{ms} = \Phi_m - \Phi_s \quad (3)$$

Where Q_{ss} is the values of the charge in the gate dielectric, Cox represents gate capacitance, Q_d denotes charge in the channel, Φ_{ms} is the metal-semiconductor work function given by the difference between the gate metal work function Φ_m and the semiconductor work function Φ_s, Φ_f represents Fermi potential, may be express as the following equation[12]:

$$\Phi_f = \frac{KT}{q} \ln \frac{NA}{Ni} \ldots \quad (4)$$

In the above equation, k represents the Boltzmann constant, T denotes the absolute temperature, q is the charge of electron, N_A is the carrier concentration of acceptor in the p-substrate, and n_i is the intrinsic charge carrier concentration. The value of kT/q is 0.02586 V at T = 300 K [13].

SIMULATION RESULTS

Nowadays, one of the most popular simulation software packages is Silvaco TCAD. The software DEVEDIT is used to construct the device by using Tonyplot 3D. The Atlas is used to simulate the structure and characteristics of the TG nFinFET device. For the simulation, we have been used Schrodinger-Poisson with Lombardi (CVT) model. The other drift-diffusion model of charge transport also used to neglect non-local effects, such as velocity overshoot and reduced energy dependent impact ionization. By specifying Shockley-Read-Hall (SRH) recombination model is activated. Similarly, we used Fermi-Dirac statistics for the simulation. [9]

The below figure shows the threshold voltage variations by using different gate materials(SiO_2, Si_3N_4, ZrO_2, HfO_2 and TiO_2) of an SOI n- FinFET of V_{DS} = 0.2 V.

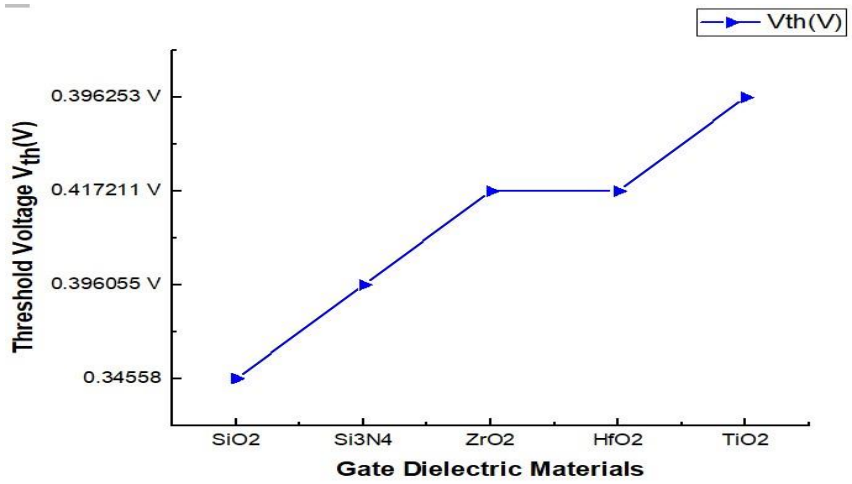

Figure 2: The Threshold Voltage V_{th} Versus Different Materials of Gate (SiO_2, Si_3N_4, ZrO_2, HfO_2 and TiO_2) of TG-FinFET.

The subthreshold swing (SS) is the important parameter which helps to calculate leakage current. The subthreshold swing is expressed as [14]

$$\text{Subthreshold swing (SS)} = \frac{dVg}{d(logId)} \text{ mV/dec} \quad (5)$$

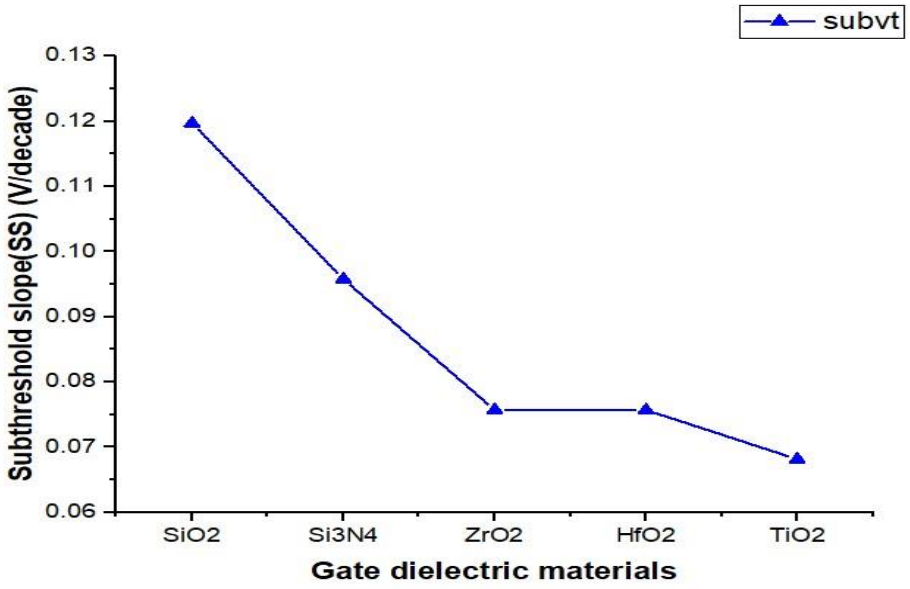

Figure 3: The Subthreshold Slope Characteristics of the TG nFinFET for Different Materials of Gate(SiO_2, Si_3N_4, ZrO_2, HfO_2 and TiO_2).

The switching performance depends on most important parameters like ON currentto OFF current ratio for SOI FinFET, and the OFF current is expressed as [15]:

$$I_{off}(\mu A) = 100\frac{W}{L}10^{\frac{-Vth}{SS}} \quad (6)$$

Where L represents channel length of the device and W denotes the width of the channel. Again the OFF state current I_{off} is extracted by calculation the drain current Id and Vds=Vdd.

Figure 4,5 and6 shows ON current, OFF current and ON/OFF current ratio for different dielectric materials (SiO_2, Si_3N_4, ZrO_2, HfO_2 and TiO_2) respectively. From the simulated graphs, we have seen that the ON current (I_{on}) is increased and leakage current or OFF current (I_{off}) decreased with the increase of the dielectric constant of the gate materials.

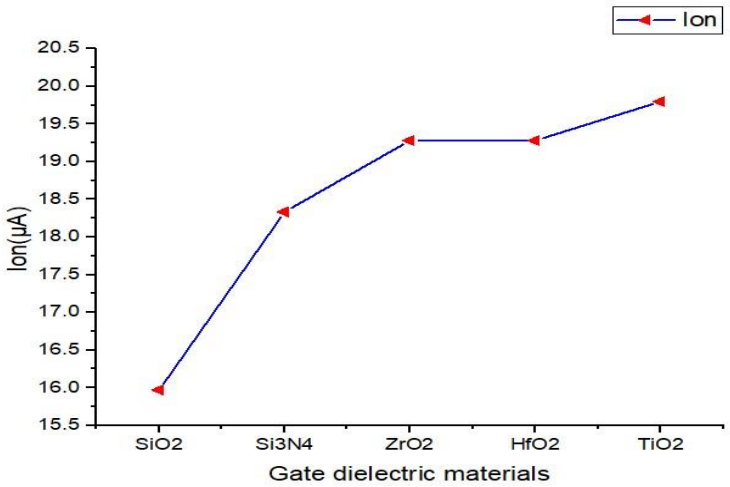

Figure 4: The Simulated Graph of ON Current and Different high k Dielectrics (SiO_2, Si_3N_4, ZrO_2, HfO_2 and TiO_2)of TG nFinFET for Vd= 0.2 V.

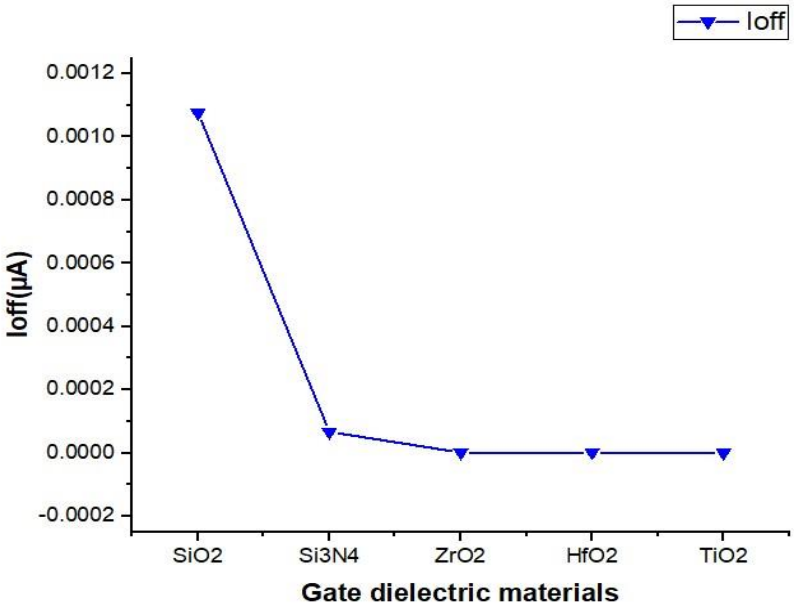

Figure 5: The Simulated Graph of OFF Current and Different High k Dielectrics (SiO_2, Si_3N_4, ZrO_2, HfO_2 and TiO_2)of TG nFinFET for Vd= 0.2 V.

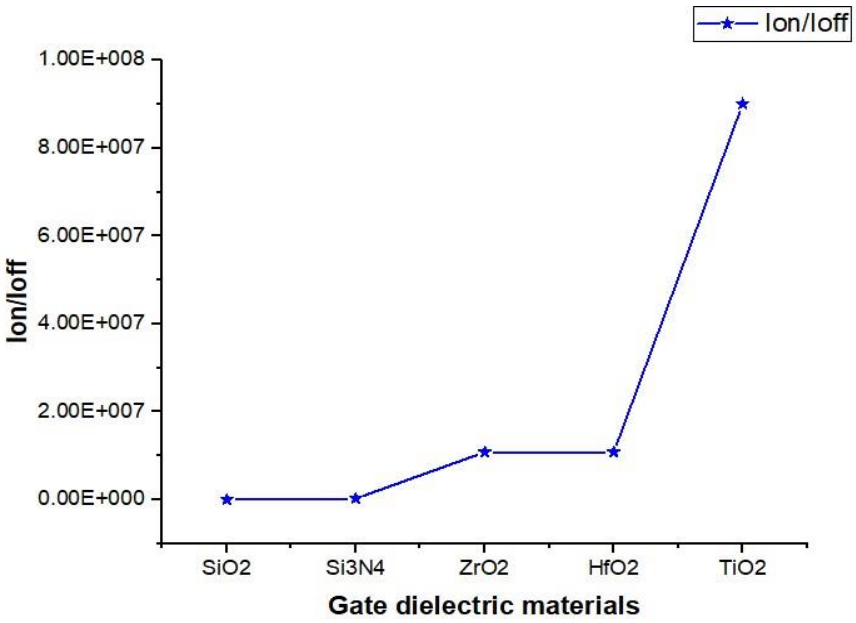

Figure 6: The ON/OFF Current Ratio of using Different Gate Materials (SiO_2, Si_3N_4, ZrO_2, HfO_2 and TiO_2) of TG-FinFET,

For a FinFET device, if effective channel length decreases and the drain voltage increases, then the drain depletion region moves closer to the source, resulting in a significant amount of electric field penetration from drain to source. For this reason, the potential barrier at the source was obtained from the increase in drain current. This process is called DIBL (drain induced barrier lowering)[16].

The electrostatics of SOI devices (well focus on DIBL, a widely used figure of merit for MOSFETs) can be captured within the following equation:

$$DIBL = 0.8\frac{\varepsilon_{si}}{\varepsilon_{ox}} \times \left(1 + \frac{T_{si}^2}{L_{el}^2}\right) \times \frac{T_{ox}}{L_{el}} \frac{T_{si} + \gamma T_{box}}{L_{el}} \times V_{ds} \quad (7)$$

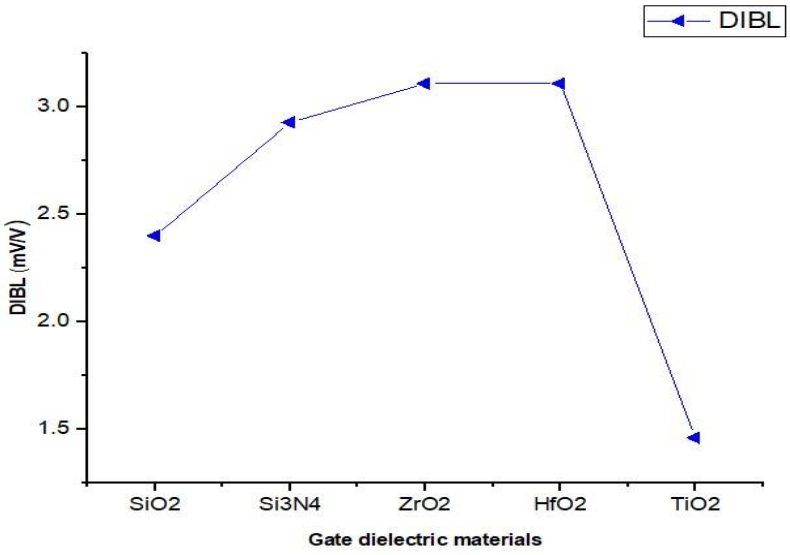

Figure 7: The DIBL Curve using Different Gate Dielectrics (SiO_2, Si_3N_4, ZrO_2, HfO_2 and TiO_2) of TG-FinFET using Vd= 0.1 to 1V.

High transconductance devices yield circuits capable of high speed operation. The calculation of transconductance is dependent on the following equation. Figure 8shows the transconductance vs gate voltage using different gate dielectric. From the figure, TiO_2 gives the maximum transconductance.

$$g_m = \frac{dID}{dVgs} \tag{8}$$

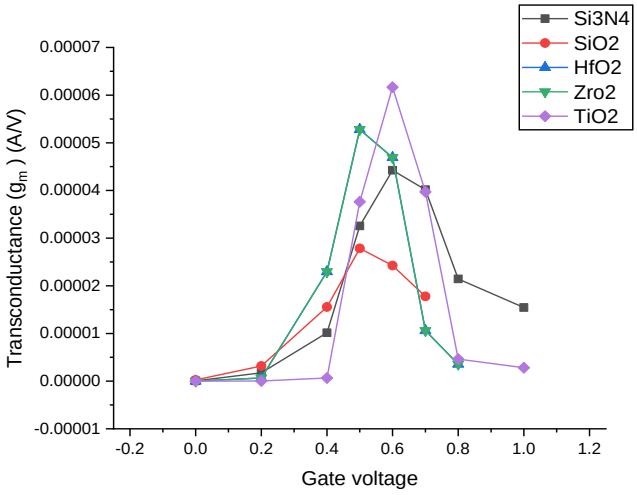

Figure 8: The Transconductance vs Gate Voltage using Different Gate Materials (SiO_2, Si_3N_4, ZrO_2, HfO_2 and TiO_2) of TG-FinFET using Vd= 0.1 to 1V.

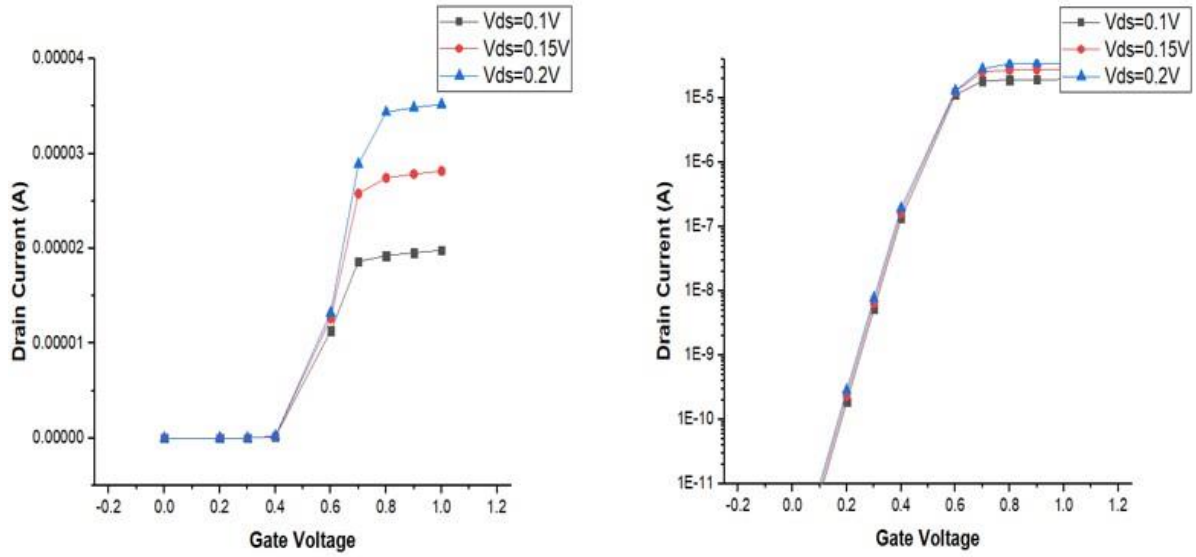

Figure 9: Simulated Graphs Oflinear Scale and Log scale of Drain Current (I_{DS}) and Gate Voltage (V_{GS}) for 5 nm TG nFinFET by using TiO_2 as a Gate Dielectric.

CONCLUSIONS

We have been simulated the electrical characteristics (TG) nFinFET with a channel length of 5nm. Different gate dielectric materials have been used in this simulation with the help of SILVACO TCAD tools. The electrical characteristics such as threshold voltage, ON current (ION), OFF current (IOFF), ratio of On-Off current, Subthreshold slope (SS), drain induced barrier lowering (DIBL) and transconductance (gm) have been simulated. After analyzing the simulations, we have seen that high permittivity (k=40) of gate material (TiO2) gives improve values of threshold voltage, subthreshold swing, ON-OFF current ratio, transconductance in comparison with other gate materials which has low dielectric constant. Finally, the high k dielectric materials have a better option in the fabrication of TG FinFET device in future.

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